REMARKS

The claims have been amended so that there are now four independent Claims 1, 2, 4 and 5. Thus the number of independent claims has been increased to a total of one more that the allowable total of three so that an additional claims fee of (1 x $210) = $210 is required. This amount is being charged to our Deposit Account.

With regard to the objections to the drawings and the table, the corrections requested by the Examiner have been entered. In the drawings these have been done by changes solely in the specification so that no changes in the drawings are entered. In the table, the changes have been entered in the table itself as these are minor and a new table is filed herewith.

With regard to the objections to the specification, the corrections requested by the Examiner have been entered.

With regard to the objections to the claims, the corrections requested by the Examiner have been entered.

With regard to the rejections to the claims under 35 U.S.C. 112, the corrections requested by the Examiner have been entered. In regard to Claim 8, the term "reference edge" appears in Claim 7 and hence it is believed that proper antecedent does exist. In regard to Claim 26, the term "increment value" now appears in the amended Claim 1 and hence it is believed that proper antecedent now exists.

With regard to the rejections to the claims under 35 U.S.C. 102 and 103, **Claim 1** has been amended as set out hereinafter and is now believed to

be properly distinguished from the prior art as stated.

The indication of allowability of **Claims 2, 4 and 5** is noted and these claims have been amended so that they are now presented as independent claims including all of the features of the claims from which they previously depended. Thus Claims 4 and 5 now include the features of original Claim 3. It is believed therefore that Claims 2, 4 and 5 are in good order for allowance.

Turning now to Claim 1, this claim has been amended to more clearly define that an arrangement generating a modulated output frequency by passing the pulses of a higher speed reference clock through digitally controlled programmable digital delay elements such that the edges of the output signal are precisely timed and phase modulated so as to produce a fixed amplitude output vector which is summed with another fixed amplitude output vector thereby producing amplitude and phase modulated QAM at the output frequency determined by the increment value.

The embodiment shown in Dress Figure 10 does not contemplate the above. Rather, Dress discloses a method wherein narrow-width time domain pulses (on the order of nanoseconds) are used to generate symbols consisting of the sum of Gaussian derivatives of said pulses. The programmable delay elements are merely used in this fashion to produce fixed Gaussian derivative order pulses from the reference pulse wherein various orders are switched on or off corresponding to the bit value of the 7-bit symbol as described in Dress column 7, lines 47 to 67. The resulting spread spectrum output is different in its

very nature from the narrowband QAM output produced by the present invention in that the Dress output is low power energy spread over a number of GHz of frequency spectrum as opposed to the typical 6 MHz channel bandwidth of QAM signals typically generated by embodiments of the present invention.

Dress further states on column 8, lines 63 to 66 that the programmable delay block is NOT used to phase modulate but rather as a mechanism to control the relative phases of the derivative pulses in a static sense. Though Dress does not disclose it in detail, it is believed that the programmable delay block 1005 simply delays the trigger pulses from the trigger generator 1002 such that properties of the output signal spectrum can presumably be tuned to some advantages. This is carried out in a static manner, i.e. while a programmable delay may be employed here, in practice it is only programmed once to fixed values according to tuned parameters. On the other hand, the delay is used for a completely different purpose in the present invention. It is used in the present invention to precisely locate the edge of the output signal relative to the reference signal edge and thereby produce a precise output frequency. The input to the programmable delay elements in the present invention is a dynamic rather than static input (the output of the high speed adder 102a) used to variably delay the edges of the reference clock such that the edges are time located where necessary to produce the desired output frequency. The delay varies for each reference clock edge by necessity whereas the delay block in Dress presumably applies static and fixed delay (once programmed for initialization and tuning) to each trigger pulse in order to produce

desired Gaussian derivative pulses.

Dress modulation block 1004 may indeed perform QAM modulation on his derivative pulses generated by block 1005 however block 1005 is NOT used to derive output frequency and phase modulation through edge control as in the present invention. The novelty of Dress lies in using Gaussian derivatives to generate advantageous spread spectrum carrier signals (derivative pulses as he calls them) which can subsequently be m-ary/QAM modulated as can any carrier signal as would be obvious to skilled artists. On the other hand, the present invention is novel in the sense that power efficiency, lower jitter, low phase noise etc is achieved. The delays of high speed reference clock pulses are constantly controlled in order to produce a resultant output signal vector that is phase modulated. Pulse shaping is not employed, only edge delay control.

Dress relies on pulse shaping to produce desirable power spectral density properties of spread spectrum carrier signals whereas the present invention improves upon the efficiency of narrowband QAM modulation by using a novel approach to generate the QAM carrier signal.

Regarding Claim 1 as amended, it is respectfully requested that the examiner consider the above that the arrangement of programmable delay applied in Dress differs materially from its use in the present invention.

Yet further the dependent claims set forth are also yet further distinguished from the prior art cited and should be allowed even if Claim 1 is rejected.

Thus regarding **Claim 3**, Wolaver (Figure 2 column 1, lines 33 to

45) does disclose an accumulator where the accumulator is clocked at the carrier frequency by the signal Vc and the resulting accumulator sum is coupled to a sine wave lookup table as is known to those skilled in the art immediately as direct digital synthesis. Further, phase modulation is added by adding Nm to the output of the accumulator before coupling to the look up table. In the present invention however, the accumulator and look up table are used rather to determine a time delay for an edge of the reference clock which is precisely timed in order to produce a desired lower output frequency with phase modulation. The use of an accumulator to delay a signal by means of programmable delay is certainly obvious to those skilled in the art, yet we believe employing a combination of the accumulator, look up table, modulation adder, and pulse swallow circuitry in order to produce QAM modulation on any output frequency lower than the reference clock frequency to be a novel approach. Moreover, the present invention seeks to improve upon prior art QAM modulation significantly by producing two fixed amplitude phase modulated vectors which are summed to produce QAM. It is the application of the accumulator, LUT, and programmable delay blocks towards this novel approach to QAM modulation that is the spirit of the present invention.

Thus regarding **Claim 6**, Dress refers to a master clock oscillator (Figure 10 block 1001, column 8, lines 56 to 63) which generates stable timing signals to control the trigger generator which determines the pulse transmission timing interval. Dress does not refer to high frequency absolute accuracy and very low phase noise performance but refers only to the master oscillator

producing stable pulses to drive his derivative pulse generators.

Thus regarding **Claim 7**, the above explanation reveals that Dress uses programmable delay in only a static fashion once the system is initialized such that he can derive his derivative Gaussian pulses from his trigger pulse. As discussed above, the present invention dynamically delays each and every edge of the reference clock input so as to produce precise edges corresponding to the desired output frequency and phase modulation.

Thus regarding **Claim 8**, this aims to specify that either the rising or falling edges of the reference clock input may be used to derive the output signal edge. Further we propose that Claim 8 be reworded to state "The apparatus according to Claim 7 wherein the reference edge of the input reference clock used to derive the edge of the output signal may be either the rising or falling edge of the input reference clock" in order to address the indefiniteness rejection.

Thus regarding **Claim 9**, this aims to specify that the exemplary embodiment of the invention as shown in Figure 2 produces the rising and falling edges of the output signal using two sets of delay elements, one handling the rising edge the other handling the falling edge thus resulting in the added advantage that duty cycle can be varied. Dress does not refer to duty cycle control and/or the impact of rising and falling edges on his derivative pulses.

Thus regarding **Claim 10**, this aims to specify that the programmable delay blocks 106a, 106b may be implemented through alteration of the input reference clock such as frequency multiplication, division, or phase shifting. Dress paragraph 63 does not refer to exemplary implementations of his

programmable delay generator 1005.

Thus regarding **Claim 11**, Wolaver (Figure 2 blocks 20 and 22 column 1, lines 32-36) uses the accumulator to drive a sine wave look up table for DDS rather than using the accumulator to drive a edge delay lookup table as in the present invention. As mentioned in the discussion regarding Claim 3, employing a combination of the accumulator, look up table, modulation adder, and pulse swallow circuitry in order to produce QAM modulation on any output frequency lower than the reference clock frequency is a novel approach. The adders and accumulators in the present invention are thus arranged in a different manner than those that would be applied in DDS in that the novel approach of the present invention deals with high frequency reference clock edges and resultant precise delay in order to generate phase modulated output signal vectors at lower frequencies.

Thus regarding **Claim 12**, Wolaver (Figure 2 blocks 20 and 22 column 1, lines 32-36) performs phase modulation by adding a modulation number Nm to the output of the accumulator whereas the present invention alters the increment value prior to coupling to the accumulator.

Thus regarding **Claim 13**, Norsworthy (Figure 3 block 318 paragraph 74) employs a sample and hold interpolator to reduce second and third order encoder quantization noise. On the other hand, in the present invention, clock and image/aliasing components of the sampled baseband spectrum are attenuated by applying (sinx)/x or linear interpolation and quantization noise is not a factor. The present invention seeks to remove the

requirement for prior art reconstruction filter as in Figure 1 by using an interpolator to attenuate and shift out clock and aliasing spectra.

Thus regarding **Claim 14**, and in view of the interpretation that Dress and Norsworthy do not disclose Claim 13, Norsworthy (Figure 3 block 318 paragraph 86) discloses that the action of his sample/hold interpolators 318 result in sinc(x) or (sinx)/x function in the frequency domain (i.e. the transfer function of a sample and hold in time domain is a sinc(x) function in frequency response as will be readily understood by those skilled in the art). In one embodiment, the present invention rather applies the (sinx)/x function in the time domain for interpolation of the baseband modulation signal. Norsworthy's sinc(x) in frequency is a result of his sample and hold in time. The present invention deliberately applies (sinx)/x in time domain to help mitigate the clock and aliasing components 402,403,404 while removing the requirement for an analog reconstruction filter.

Thus regarding **Claim 15**,, and in view of the interpretation that Dress and Norsworthy do not disclose Claim 13, Berangi (paragraph 87) does disclose that the requirements of the reconstruction filter can be relaxed through the use of an interpolation filter. The present invention eliminates the analog reconstruction filter entirely by employing interpolation in a manner aimed at maximally attenuating clock and aliasing components resulting from sampling of the baseband modulation signal and also shifting them out in frequency. Claim 15 conveys that the digital interpolation avoids the necessity of reconstruction filters.

Thus regarding **Claim 16**, Norsworthy (Figure 3 block 312 and 318 paragraph 60 – 61 and 74 - 75) discloses interpolators for sample rate conversion which are sample and hold based. The present invention employs linear or (sinx)/x interpolation for improved performance.

Thus regarding **Claim 17**, Nakagawa (Figure 8 column 2, lines 13 - 53) describes a prior art "pulse swallow counter" which uses two programmable counters 21 and 22 to switch the division ration of divider 23 from P+1 to P and back again repetitively. While named as such, the architecture described in Nakagawa Figure 8 doesn't ignore/swallow one or many edges of the input reference clock as in the present invention. Nakagawa simply derives an average division ration by using the Figure 8 architecture. Nakagawa does not refer actually to ignoring or swallowing one or many input edges.

Thus regarding **Claim 18**, Nakagawa (Figure 8 column 2, lines 13 - 53) again describes a prior art "pulse swallow counter" which uses two programmable counters 21 and 22 to switch the division ration of divider 23 from P+1 to P and back again repetitively. While named as such, the architecture described in Nakagawa Figure 8 doesn't ignore/swallow one or many edges of the input reference clock as in the present invention with a possible result that multiple reference clock pulses can be ignored/blocked in order to produce any lower output frequency by noting the carry (overflow) bits of the adder/accumulator math. Nakagawa uses the counters 21 and 22 to repeatedly switch his divider 23 from P+1 to P to produce a resultant Pave divider ratio. The

present invention uses accumulator carry bits to block one or more reference clock edges to produce delay extending over multiple cycles of the reference clock if necessary.

Thus regarding **Claim 20**, Wolaver (Figure 2 block 24 column 1, lines 32 - 46 and Figures 10 and 15 block 78 column 7, line 30 to column 8, line 6) presents a mathematical method of determining edge positions whereas Claim 20 of the present invention aims to specify that the look up tables 105a and 105b are calibrated empirically to provide 360 degrees of phase delay over a range of numbers (as output from the accumulator) from 0 to $2^n$ when their output is applied to the programmable delay elements.

Thus regarding **Claim 21**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 20, Wolaver (Figure 2 blocks 20 and 22 column 1, lines 32 - 36 and column 10, line 66 to column 11, line 7) forgoes temperature compensation by employing a ring oscillator architecture however it is unclear how the requirement for temperature compensation is avoided presuming that like any other circuitry the delay elements 356a through 356d of figure 25 in Wolaver would be subject to temperature variation. Claim 21 of the present invention directly specifies that temperature compensation is achieved by using multiple sets of lookup tables calibrated over temperature in an empirical manner.

Thus regarding **Claim 22**, Wolaver (Figure 14 block 88 column 8, lines 38 - 56) employs a D flip-flop in a sequential logic architecture such that the AND gates 84a and 84b are alternately used to allow the outputs of the

programmable delay lines 74a and 74b to reach the output Vo. This multiplexes two different delay edges from the input Vi onto the output. The present invention uses a flip-flop not for multiplexing but to provide duty cycle control according to delay elements 106a and 106b which respectively set and reset the output of the flip-flop thereby applying desired duty cycle to the output 150.

Thus regarding **Claim 23**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 22, Wolaver (Figure 2 blocks 20 and 22 column 1, lines 32 - 46 and column 10, line 66 to column 11, line 7) refers only to using the output of the accumulator to drive a sine-wave lookup table and does not examine duty cycle implications when dealing with square waves. The present invention achieves duty cycle control by initializing the accumulators 111a 111b such that the rising and falling edges of the output are a fixed time apart.

Thus regarding **Claim 24**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 22, Wolaver (Figure 12 and 13 column 8, lines 16 - 29) simply states that it is convenient for the duty cycle of the input Vi to be 50% whereas Claim 24 of the present invention conveys that the input duty cycle can be any value while the output duty cycle can be controlled to any value, typically 50%.

Thus regarding **Claim 25**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 13, Park (Figure 2 block 223 column 6, lines 10 - 14) applies predistortion in order to use non-linear amplifiers whereas the present invention requires no such predistortion since amplitude of the output

vectors 150, 154 is not modulated. The amplitude modulation component of QAM is achieved by summing the phase modulated vectors 150, 154 in block 152. Those skilled in the art will understand that all power amplifiers are non-linear in nature. In prior art there are two alternatives to mitigate the non-linearity. The first is to "back off" or only operate the power amplifier in its linear range. This is inefficient as the peak power of the amplifier is typically significantly higher then the max linear power and thus power is wasted. The other alternative is to predistort as in Park so as to compensate for the non-linearity by applying shaping to the signal prior to amplification matching the inverse of the amplifier's non-linearity characteristic. The novel approach to QAM modulation in the present invention allows the system to use the entire linear and non-linear range of the power amplifier without predistortion as amplitude modulation does not yet exist at the point of power amplification.

Thus regarding **Claim 26**, and in view of the interpretation that Dress does not disclose Claim 8, Dress paragraph 63 does not refer to an increment value or that a single increment value can be used to derive both the rising and falling edges of the output signal. While a clock inherently does have rising and falling edges, Claim 26 aims to specify that a common increment value is used to control both the rising and falling edges in a precise manner. Further we propose that claim 26 be reworded to state "The apparatus according to Claim 8 wherein the increment value of the accumulators used to drive the lookup tables for the rising and falling edges is common to both the rising and falling edge sections" in order to address the indefiniteness rejection.

Thus regarding **Claim 28**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 3, Wolaver (Figure 12 and 13 column 7, lines 34 - 43) refers to fine and coarse resolution control through equation 2. Wolaver does not refer to increasing the frequency resolution by increasing the number of binary bits in the adder math as in Claim 28 of the present invention. Wolaver Equation 2 merely points out how the two grades of resolution (coarse and fine) values are calculated and does not imply increasing resolution in any manner. Moreover, Wolaver states that the resolution is fixed as T = 1/fc.

Thus regarding **Claim 29**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 3, Wolaver (Figure 12 and 13 column 7, lines 34 – 43) again states that resolution is fixed as T = 1/fc and does not refer to using higher numbers of bits in the adder math in order to achieve more precise resolution. Claim 29 of the present invention aims to convey that an embodiment of the invention may add more bits of resolution to the adder/accumulator and subsequently truncate the least significant bits before presenting the output to the look up tables. This allows the adder/accumulator math to be carried out more precisely.

Thus regarding **Claim 30**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 3, Dress (Figure 10 block 1004 paragraph 62) does discuss using 7 separate parallel path signals to derive his 7 derivative-order pulses. This differs from the aim of Claim 30 of the present invention which aims to convey that alternatively, in another embodiment of the

present invention, parallel processing can be applied in the adders and accumulators to increase the speed. Dress refers to parallel paths for each of his 7 derivative signals but not to increasing performance through parallel processing within adder/accumulator blocks as in Claim 30.

Thus regarding **Claim 31**, and in view of the interpretation that Dress and Wolaver do not disclose Claim 3, Wolaver (Figure 12 and 13 column 7, lines 34 - 43) discloses a look up table with values calculated for his fine and coarse resolution numbers N1n and N2n but does not speak to implementation of adders and accumulators using larger look up tables. Wolaver still employs discrete blocks for a differentiator 56 and summer 55, as well as a count down circuit 54. Claim 31 of the present invention aims to specify that one large look up table with precomputed answers comprising the net effect of the modulation adder 120, accumulators 102a, 102b, and look up tables 105a, 105b is stored in memory for a particular increment value such that every edge of the input reference clock simply references the next entry of the large lookup table to provide delay control to the programmable delay 106a, 106b and pulse swallow 104a, 104b. Further we propose that Claim 31 be reworded to state "The apparatus according to Claim 3 wherein the programmable digital delay elements are arranged such that the adders/accumulators can be implemented in a larger lookup table wherein all possible output values of the modulation adder and high speed adders/accumulators for a given increment value are precomputed and stored" in order to address the indefiniteness rejection.

It is submitted therefore that the application is in good order for allowance.

Respectfully submitted

GERALD HARRON ET AL

PER:
Adrian D. Battison
Registration No: 31,726

ADB/ll
February 28, 2008
Enc.(1)

Adrian D. Battison Winnipeg, Manitoba, Canada
Telephone (204) 944-0032 - FAX (204) 942-5723